DATA SHEET

74LV4040

12-stage binary ripple counter

Product specification

1998 Jun 23

IC24 Data Handbook

Philips
Semiconductors

PHILIPS

12-stage binary ripple counter   74LV4040

FEATURES

- Optimized for Low Voltage applications: 1.0 to 5.5V

- Accepts TTL input levels between $V_{CC} = 2.7V$ and $V_{CC} = 3.6V$

- Typical V_{OLP} (output ground bounce) $< 0.8V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25°C$

- Typical V_{OHV} (output V_{OH} undershoot) $> 2V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25°C$

- Frequency dividing circuits

- Time delay circuits

- Control counters

- Output capability: standard

- I_{CC} category: MSI

DESCRIPTION

The 74LV4040 is a low–voltage Si–gate CMOS device and is pin and function compatible with 74HC/HCT4040.

The 74LV4040 is a 12-stage binary ripple counter with a click input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0 to Q_{11}). The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25°C$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1} MR to Q_n	$C_L = 15pF$ $V_{CC} = 3.3V$	12 7 16	ns
f_{max}	Maximum clock frequency		100	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	30	pF

NOTES:
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	−40°C to +125°C	74LV4040 N	74LV4040 N	SOT38-4
16-Pin Plastic SO	−40°C to +125°C	74LV4040 D	74LV4040 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +125°C	74LV4040 DB	74LV4040 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +125°C	74LV4040 PW	74LV4040PW DH	SOT403-1

12-stage binary ripple counter
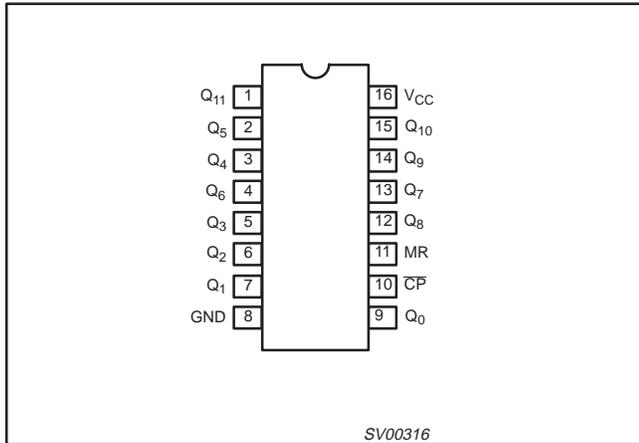
74LV4040

PIN CONFIGURATION

Figure 1. Pin configuration

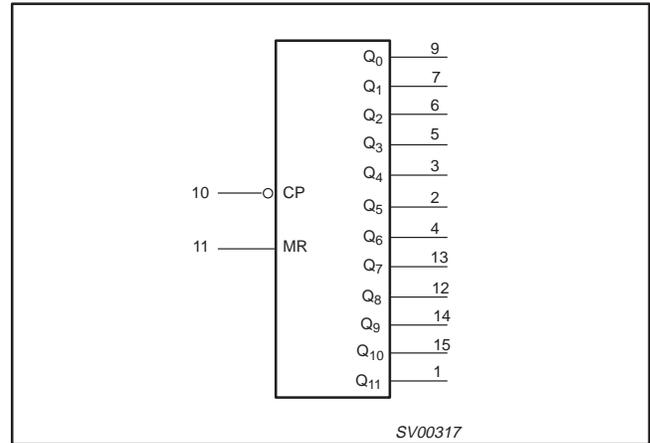## PIN DESCRIPTION

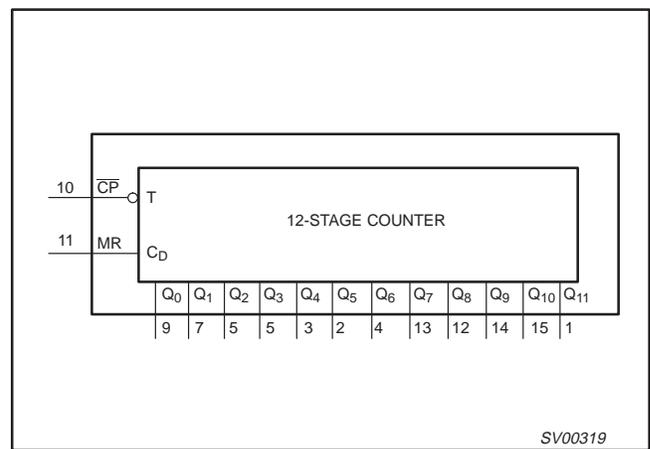| PIN NUMBER	SYMBOL	FUNCTION
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q_0 to Q_{11}	Parallel outputs
8	GND	Ground (0V)
10	$\overline{CP}$	Clock input (HIGH-to-LOW, edge-triggered)
11	MR	Master reset input (active HIGH)
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)

Figure 2. IEC Logic symbol

LOGIC SYMBOL

Figure 3. Logic symbol

FUNCTIONAL DIAGRAM

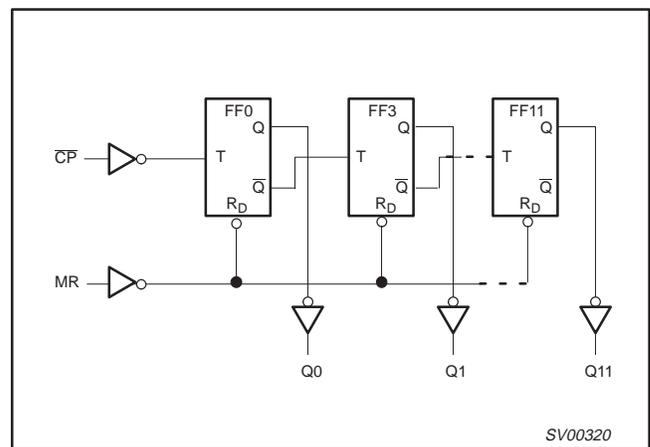**Figure 4. Functional diagram**

LOGIC DIAGRAM

Figure 5. Logic diagram

12-stage binary ripple counter

74LV4040
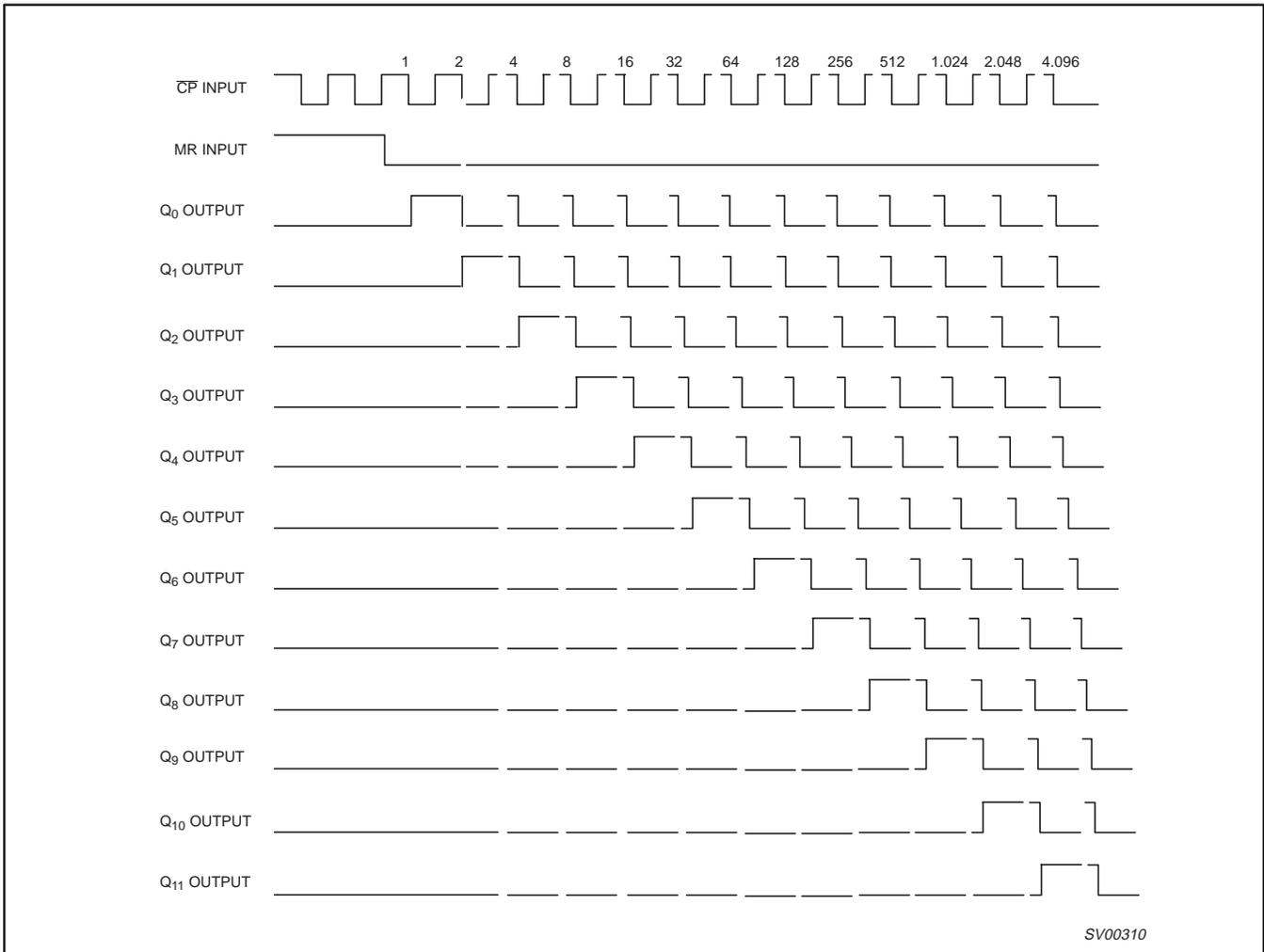
Figure 6. Timing diagram

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_0, Q_3 to Q_{13}
↑	L	no change
↓	L	count
X	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW -to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

12-stage binary ripple counter

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

12-stage binary ripple counter

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	$V_{CC} = 1.2V$	0.9			0.9		V
		$V_{CC} = 2.0V$	1.4			1.4		
		$V_{CC} = 2.7$ to $3.6V$	2.0			2.0		
		$V_{CC} = 4.5$ to $5.5V$	$0.7*V_{CC}$			$0.7*V_{CC}$		
V_{IL}	LOW level Input voltage	$V_{CC} = 1.2V$			0.3		0.3	V
		$V_{CC} = 2.0V$			0.6		0.6	
		$V_{CC} = 2.7$ to $3.6V$			0.8		0.8	
		$V_{CC} = 4.5$ to 5.5			$0.3*V_{CC}$		$0.3*V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	$V_{CC} = 1.2V$; $V_I = V_{IH}$ or V_{IL}; $-I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0V$; $V_I = V_{IH}$ or V_{IL}; $-I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL}; $-I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL}; $-I_O = 100\mu A$	2.8	3.0		2.8		
		$V_{CC} = 4.5V$; $V_I = V_{IH}$ or V_{IL}; $-I_O = 100\mu A$	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL}; $-I_O = 6mA$	2.40	2.82		2.20		V
		$V_{CC} = 4.5V$; $V_I = V_{IH}$ or V_{IL}; $-I_O = 12mA$	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	$V_{CC} = 1.2V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0				V
		$V_{CC} = 2.0V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 4.5V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 6mA$		0.25	0.40		0.50	V
		$V_{CC} = 4.5V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 12mA$		0.35	0.55		0.65	
I_I	Input leakage current	$V_{CC} = 5.5V$; $V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; MSI	$V_{CC} = 5.5V$; $V_I = V_{CC}$ or GND; $I_O = 0$			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	$V_{CC} = 2.7V$ to $3.6V$; $V_I = V_{CC} -0.6V$			500		850	μA

NOTE:
1. All typical values are measured at $T_{amb} = 25°C$.

12-stage binary ripple counter

74LV4040

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS −40 to +85 °C			LIMITS −40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $\overline{CP}$ to Q_0	Figure 7, 9	1.2	–	60	–	–	–	ns
			2.0	–	27	43	–	54	
			2.7	–	19	31	–	38	
			3.0 to 3.6	–	16[2]	26	–	32	
			4.5 to 5.5	–	11[3]	17	–	22	
t_{PHL}/t_{PLH}	Propagation delay Q_n to Q_{n+1}	Figure 7, 9	1.2	–	40	–	–	–	ns
			2.0	–	18	29	–	54	
			2.7	–	13	21	–	38	
			3.0 to 3.6	–	11[2]	18	–	32	
			4.5 to 5.5	–	7[3]	12	–	22	
t_{PHL}	Propagation delay MR to Q_n	Figure 8, 9	1.2	–	55	–	–	–	ns
			2.0	–	27	44	–	54	
			2.7	–	19	31	–	38	
			3.0 to 3.6	–	16[2]	26	–	32	
			4.5 to 5.5	–	11[3]	17	–	22	
t_W	Clock pulse width HIGH to LOW	Figure 7	2.0	35	7	–	41	54	ns
			2.7	25	5	–	30	–	
			3.0 to 3.6	20	4[2]	–	24	–	
			4.5 to 5.5	15	3[3]	–	18	–	
t_W	Master reset pulse width HIGH	Figure 8	2.0	35	11	–	41	–	ns
			2.7	25	9	–	30	–	
			3.0 to 3.6	20	8[2]	–	24	–	
			4.5 to 5.5	15	7[3]	–	18	–	
t_{rem}	Removal time MR to CP	Figure 8	1.2	–	10	–	–	–	ns
			2.0	22	5	–	26	–	
			2.7	16	4	–	19	–	
			3.0 to 3.6	13	3[2]	–	15	–	
			4.5 to 5.5	10	2[3]	–	12	–	
f_{max}	Maximum clock pulse frequency	Figure 7	2.0	14	60	–	12	–	MHz
			2.7	19	76	–	16	–	
			3.0 to 3.6	24	94[2]	–	20	–	
			4.5 to 5.5	36	112[3]	–	30	–	

NOTES:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25°C$.

2. Typical value measured at $V_{CC} = 3.3$V.

3. Typical value measured at $V_{CC} = 5.0$V.

12-stage binary ripple counter

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq 2.7V \leq 3.6V$
V_M = 0.5V * V_{CC} at $V_{CC} < 2.7V$ and $\geq 4.5V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

SV00322
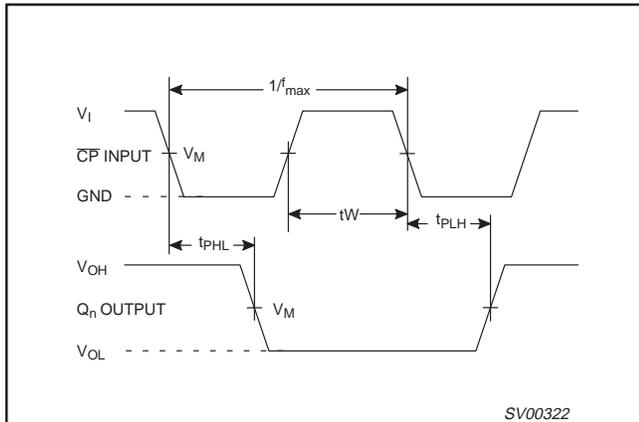
Figure 7. Clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency

SV00908
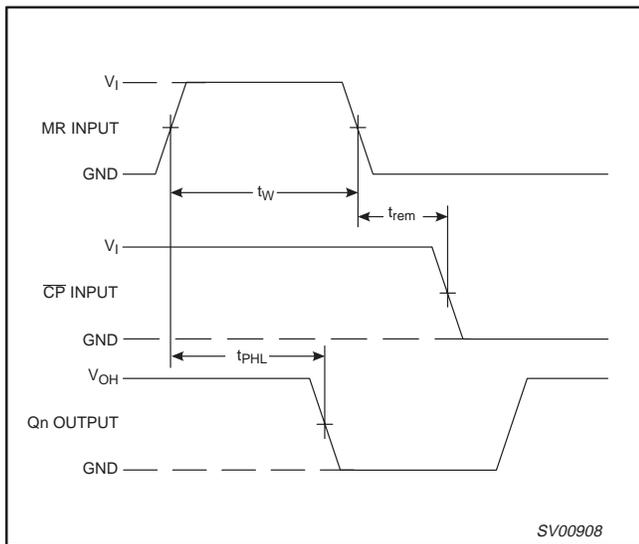
Figure 8. Master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time

TEST CIRCUIT

Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V

SV00901

Figure 9. Load circuitry for switching times

12-stage binary ripple counter

74LV4040

DIP16: plastic dual in-line package; 16 leads (300 mil)   **SOT38-4**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

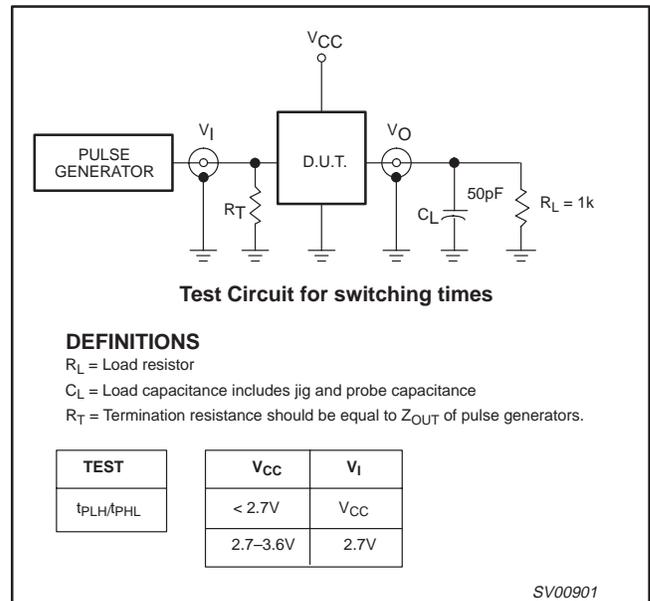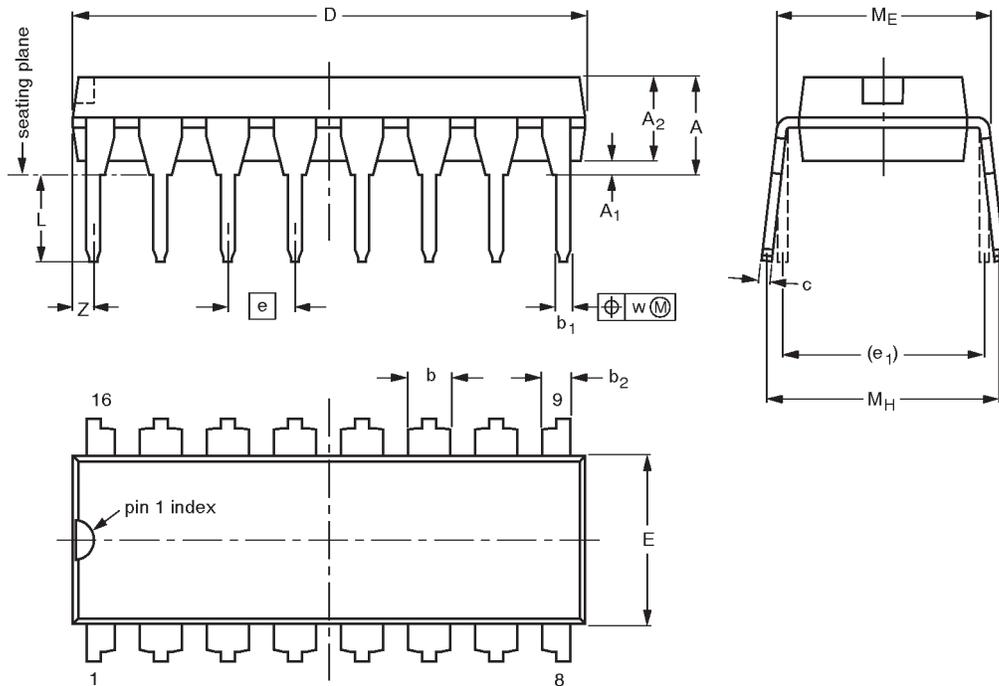| UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
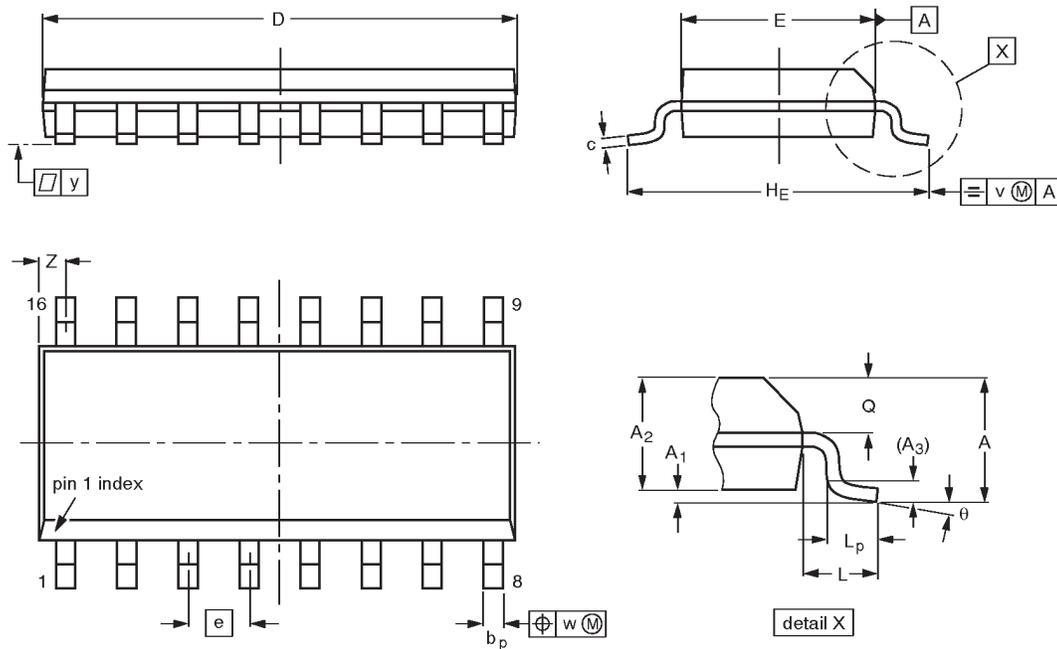
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

12-stage binary ripple counter

74LV4040

SO16:   plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	Hₑ	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

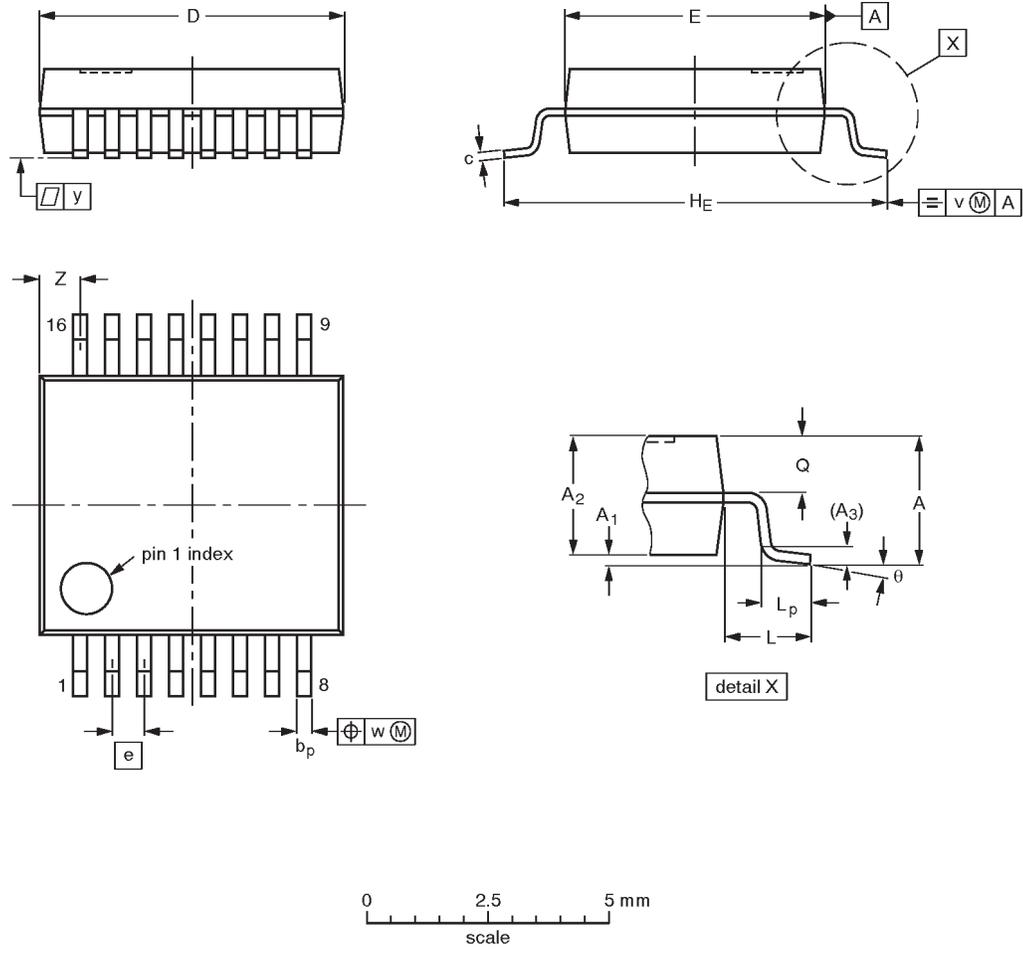1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

12-stage binary ripple counter

74LV4040

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

0   2.5   5 mm
scale

pin 1 index

detail X

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

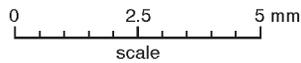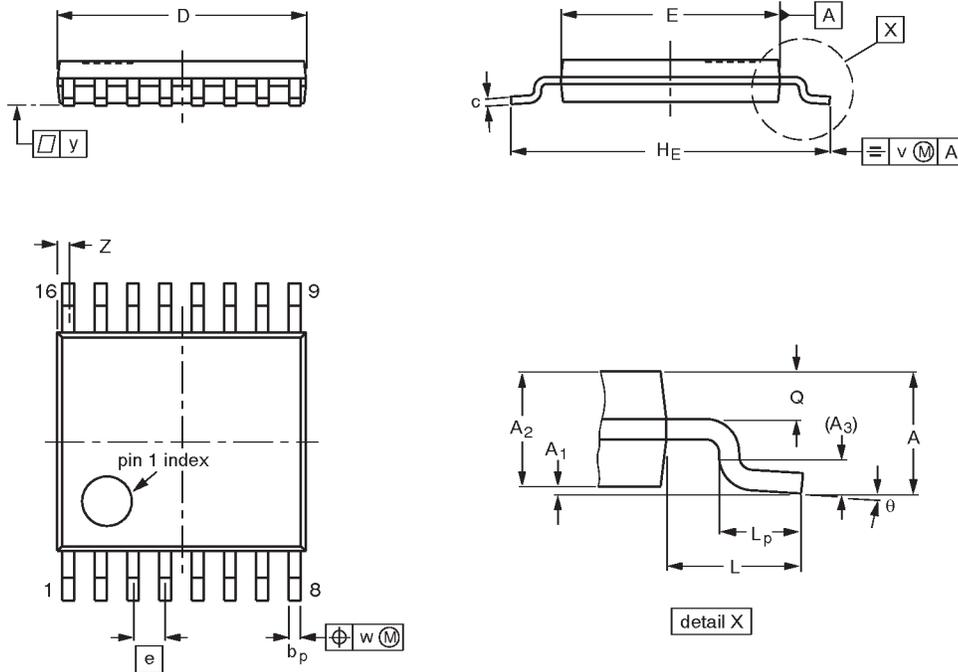1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14 95-02-04

12-stage binary ripple counter

74LV4040

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1

0   2.5   5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D [1]	E [2]	e	Hₑ	L	Lₚ	Q	v	w	y	Z [1]	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Let's make things better.

Philips
Semiconductors

PHILIPS